What is claimed is:

1. A semiconducting device comprising:

a substrate;

a first die attached to the substrate, the first die including active circuitry on an upper surface;

a spacer covering the active circuitry on the upper surface of the first die, the spacer extending from a first side of the first die to an opposing second side of the first die and extending near a third side of the first die and an opposing fourth side of the first die such that the active circuitry is exposed near the third and fourth sides of the first die; and

a second die stacked onto the spacer and the first die.

2. The semiconducting device of claim 1, wherein the active circuitry on the upper surface of the first die includes a flash memory array.

3. The semiconducting device of claim 1, wherein the spacer is attached to the upper surface of the first die using an adhesive.

4. The semiconducting device of claim 1, wherein the spacer includes at least one section that extends to the third side of the first die such that the active circuitry is only partially exposed near the third side of the first die.

5. The semiconducting device of claim 4, wherein the spacer includes at least one section that extends to the fourth side of the first die such that the active circuitry is only partially exposed near the fourth side of the first die.

6. The semiconducting device of claim 1, wherein the spacer is about 1mm away from the third and fourth sides of the first die.

7. The semiconducting device of claim 1, wherein the spacer is formed of silicon.

8. The semiconducting device of claim 1, further comprising at least one additional die stacked onto the first die, the spacer and the second die.

9. The semiconducting device of claim 1, further comprising at least one additional die mounted on the substrate, the first die being stacked onto the at least one additional die.

10. The semiconducting device of claim 1, wherein the second die is attached to the spacer using an adhesive.

11. The semiconducting device of claim 1, further comprising wires bonded to pads that are part of the exposed active circuitry near the third and fourth sides of the first die.

12. A method comprising:

securing a first die to a substrate, the first die including active circuitry on an upper surface;

covering the active circuitry on the upper surface of the first die with a spacer that extends from a first side of the first die to an opposing second side of the first die, the spacer extending near a third side of the first die and an opposing fourth side of the first die such that the active circuitry is exposed near the third and fourth sides of the first die; and

stacking a second die onto the spacer and the first die.

13. The method of claim 12, wherein stacking the second die onto the spacer and the first die includes securing the second die to the spacer with an adhesive.

14. The method of claim 12, further comprising stacking at least one additional die onto the second die.

15. The method of claim 12, further comprising securing at least one additional die between the first die and the substrate.

16. The method of claim 12, wherein covering the active circuitry on the first die with a spacer includes covering the active circuitry where at least one section of the spacer extends to the third side of the first die such that only a portion of the active circuitry is exposed near the third side of the first die.

17. The method of claim 16, wherein covering the active circuitry on the first die with a spacer includes covering the active circuitry where at least one section of the spacer extends to the fourth side of the first die such that only a portion of the active circuitry is exposed near the fourth side of the first die.

18. The method of claim 12, wherein covering the active circuitry such that the spacer extends near a third side of the first die and a fourth side of the first die includes covering the active circuitry such that the spacer is about 1mm away from the third and fourth sides of the first die.

19. The method of claim 12, wherein covering the active circuitry on the first die with a spacer includes attaching the spacer to the active circuitry with an adhesive.

20. The method of claim 12, wherein covering the active circuitry on the first die with a spacer includes covering a portion of a flash memory array on the first die with the spacer.

21. The method of claim 12, further comprising bonding wires to pads that are part of the exposed active circuitry near the third and fourth sides of the first die.

22. An electronic system comprising:

a buss;

a memory coupled to the buss; and

a semiconducting device that is electrically connected to the buss, the semiconducting device including a substrate and a flash memory that is attached to the substrate, the flash memory including active circuitry on an upper surface, the semiconducting device further including a spacer covering the active circuitry on the upper surface of the flash memory and a die that is stacked onto the spacer and the flash memory, the spacer extending from a first side of the flash memory to an opposing second side of the flash memory and extending near a third side of the flash memory and an opposing fourth side of the flash memory such that the active circuitry is exposed near the third and fourth sides of the flash memory.

23. The electronic system of claim 22, wherein the spacer includes at least one section that extends to the third side of the flash memory such that the active circuitry is only partially exposed near the third side of the flash memory.

24. The electronic system of claim 23, wherein the spacer includes at least one section that extends to the fourth side of the flash memory such that the active circuitry is only partially exposed near the fourth side of the flash memory.

25. The electronic system of claim 22, further comprising a voltage source electrically coupled to the semiconducting device.

26. The electronic system of claim 22, further comprising wires bonded to pads that are part of the exposed active circuitry near the third and fourth sides of the flash memory, the wires being electrically coupled to the substrate.